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WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
WANG, JIN CHENG	
ART UNIT	PAPER NUMBER
2628	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/724,197	GETTEMY ET AL.	
	Examiner	Art Unit	
	Jin-Cheng Wang	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-14 and 16-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-14 and 16-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/16/2007 has been entered. Claims 1, 4, 10, and 18 have been amended. Claims 7 and 15 have been canceled. Claims 1-6, 8-14 and 16-23 are pending in the application.

Response to Arguments

Applicant's arguments filed on February 16, 2007 has been considered, but are not found persuasive in view of the prior art of record. As addressed below, the cited references teach the claim limitations set forth in the claim 1.

Matsuzaki teaches a display unit (e.g., figures 1-2) comprising:

A display panel comprising a pixel matrix comprising: a rectangular pixel frame buffer region (e.g., figures 6-7B; column 5, lines 25-60);

A fixed, active pixel border region permanently dedicated to displaying a border attribute, wherein said fixed, active pixel border region surrounds said rectangular pixel frame buffer region and comprises a width of less than 256 pixels (e.g., figures 6-7B; column 5, lines 25-60);

A frame buffer memory (VRAM 22) for containing image data for generating an image within said frame buffer region (figures 6-7B; column 5, lines 25-60);

A display controller (e.g., the display control circuit, SVGA 21 of figure 3) coupled to said frame buffer memory (e.g., VRAM 22), coupled to receive said border attribute from said border attribute register (e.g., the border producing circuit or registers of figures 1-3; column 5, lines 5-60; column 7, lines 10-65), and coupled to control said display panel (figures 1-7B; column 5, lines 5-60), said display controller for generating a first set of signals (i.e., pixel data) for rendering said image within said frame buffer region and for generating a second set of signals (i.e., border pixel data) for displaying said display attribute within said fixed, active pixel region (e.g., column 3, lines 6-25; column 7, lines 5-67; column 8, lines 1-35; column 13, lines 48-60).

However, it is remains to be shown whether Matsuzaki explicitly teaches a frame buffer memory. Matsuzaki teaches a VRAM for storing a frame of the image data (*Matsuzaki column 2, lines 10-15*) and a graphics control circuit fetching pixel data from VRAM 22 (*Matsuzaki figures 1-3; column 6, lines 3-65*) wherein VRAM 22 is a frame buffer memory.

It remains to be shown whether Matsuzaki teaches a border attribute register dedicated for containing said border attribute, wherein said border attribute is automatically selected to provide viewing contrast with image data located near said border region, and wherein said border attribute comprises color information for each pixel in said fixed, active pixel border region, and wherein said border attribute is equal to a background attribute currently being displayed.

Matsuzaki teaches selecting/switching one of the display formats including resolutions (*Matsuzaki column 2*); setting the format of the binary border pixel data in color values for the border pixels to be different from those for pixels within the effective display region (*Matsuzaki column 3 and 6-7*) and the format of the synthesized pixel data in the border section produced as 8-bit parallel data by the border producing circuit 25 synthesized with the pixel data from the

binarizing half tone processing circuit 26 by the synthesizing circuit 27 (Matsuzaki column 3, 6-7) and therefore suggesting an obvious modification of Matsuzaki.

Matsuzaki teaches selecting/switching one of the display formats including resolutions (Matsuzaki column 2); setting the format of the binary border pixel data in **color values (color intensities) for the border pixels** to be different from those for pixels within the effective display region (Matsuzaki column 3 and 6-7) and thereby selecting the color values for the border area pixels surrounding the frame area image data to provide the viewing contrast. It is noted that in Matsuzaki, the color values for the border area pixels is *automatically selected by the selecting/switching mechanism* to provide viewing contrast.

Kim teaches implicitly a frame buffer (*See Kim column 8, lines 55-67*). Furthermore, Singla teaches a display attribute being selected to provide viewing contrast with image data located near the border region (*e.g., Singla column 3, lines 28-50; column 5, lines 45-60*).

It would have been obvious to one of ordinary skill in the art to have incorporated the Kim's frame buffer and Singla's border region attribute setting method into Matsuzaki's display unit because Matsuzaki teaches a VRAM for storing image data (*Matsuzaki column 2, lines 10-15*) and a graphics control circuit fetching pixel data from VRAM 22 (*Matsuzaki figures 1-3; column 6, lines 3-65*) while Kim teaches a VRAM corresponds to a frame buffer memory (region). Moreover, Matsuzaki teaches selecting/switching one of the display formats including resolutions (*Matsuzaki column 2*); setting the format of the binary border pixel data in color values for the border pixels to be different from those for pixels within the effective display region (*Matsuzaki column 3 and 6-7*) and the format of the synthesized pixel data in the border section produced as 8-bit parallel data by the border producing circuit 25 synthesized with the

pixel data from the binarizing half tone processing circuit 26 by the synthesizing circuit 27 (Matsuzaki column 3, 6-7) and therefore suggesting an obvious modification of Matsuzaki.

One having the ordinary skill in the art would have been motivated to incorporate the frame buffer of Kim because Kim teaches that the video frame buffer memory is constructed from VRAM (See Kim column 8, lines 55-67). One of the ordinary skill in the art would have been motivated to incorporate Singla's border region attribute setting method because Singla teaches a set of registers associated with a timing generator programmed to a particular attribute including resolution (selectable resolution; Singla the Abstract column 5) and Singla further teaches border data set by a solid single-color surrounding the frame buffer image (changeable color; Singla column 8) and a display controller for user-selectable overriding of the predetermined border scheme to provide viewing contrast between the border region and the frame buffer region (changeable attributes; e.g., Singla the Abstract and column 10).

Although Matsuzaki, Kim and Singla does not explicitly disclose the claim limitation of "said display attribute is *automatically* selected to provide viewing contrast with image data located near said border region, wherein said display attribute comprises color and intensity information, and wherein said display attribute is equal to a background attribute", Dinwiddie discloses in column 9, lines 30-40 that the color data signal from the fringe palette 100 is *automatically* selected to provide the color for the fringe area around the OSD frame area and thereby the fringe color provides viewing contrast for the frame area. Moreover, Dinwiddie also discloses in column 11, lines 25-67 selecting a solid color byte from the fringe palette to provide the fringe color data for the fringe area surrounding the OSD frame area and controlling the extra bits to finger palettes and/or the attribute buffer with those extra bits controlling appropriate

circuitry in the OSD system to generate those attributes. Therefore, Dinwiddie discloses the claim limitation of the display attribute being *automatically* selected to provide viewing contrast with image data (in the frame area).

Dinwiddie discloses in column 8, line 65 to column 9, line 18 that the attribute a ten bit entry from the fringe palette which produces a fringe color data signal containing three color component signals having three bits. The fringe palette of 512 colors (column 10, lines 5-15), each of the RGB intensities are represented by an 3-bit value. Therefore, Dinwiddie discloses the claim limitation that the display attribute comprises color and intensity information (See also column 11, lines 61-65).

Dinwiddie discloses in column 10, lines 5-15 that background colors are selected from 512 possible colors and one fringe color is also selected from 512 possible colors. In addition, each palette entry in the foreground palette 42', the background palette 44' and the fringe palette 100 may be specified to appear as a solid color or a transparent overlay atop the received television image.

Applicant's claim limitation of "a background attribute" is any attribute, e.g., or a color attribute out from the 512 possible colors. Since Dinwiddie discloses one fringe color selected from the 512 possible colors, Dinwiddie has taught the fringe attribute being equal to one of the background attributes. Moreover, Dinwiddie discloses in column 11, lines 28-31 that the fringe palette 100 contains a single one byte entry corresponding to the portion of the palette 40" entry containing the background data, which contains a color data signal C and a solid color bit S. The solid color bit S, as selected from the 512 colors, is equal to one of the background solid color bit BG S, which is also selected from the same 512 colors.

Moreover, Matsuzaki suggests the claim limitation because Matsuzaki teaches selecting/switching one of the display formats including resolutions (Matsuzaki column 2); setting the format of the binary border pixel data in **color values (color intensities) for the border pixels** to be different from those for pixels within the effective display region (Matsuzaki column 3 and 6-7) and thereby selecting the color values for the border area pixels surrounding the frame area image data to provide the viewing contrast. It is noted that in Matsuzaki, the color values for the border area pixels is *automatically selected by the selecting/switching mechanism* to provide viewing contrast.

Singla discloses border data set by a solid single-color surrounding the frame buffer image (changeable color; Singla column 8) and a display controller for user-selectable overriding of the predetermined border scheme to provide viewing contrast between the border region and the frame buffer region (changeable attributes; e.g., Singla the Abstract and column 10). Although Singla incorporates a user-selectable overriding of the border color data, the border color attribute is still being automatically selected by the display controller because once the user provides the color data, the display controller automatically selects the border color data to provide viewing contrast to the frame area image data.

One of the ordinary skill in the art would have been motivated to have *automatically* selected the border color attribute because it allows for the border color attribute to be set by the computer software and hardware in which the format of the binary border pixel data in color values for the border pixels is set to be different from those for pixels within the effective display region (Matsuzaki column 3 and 6-7) to provide viewing contrast and to provide changeable

attribute to the border area pixels to provide controllable color attribute for the border region (Singla the Abstract and column 10).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 10 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yuki et al. U.S. Patent No. 5,805,149 (hereinafter Yuki).

Re Claims 1, 10 and 18:

Yuki teaches a display unit (e.g., figure 4) comprising:

A display panel comprising a pixel matrix (e.g., Figs. 3(a)-3(b) and column 5, lines 35-45) comprising:

A rectangular pixel frame buffer region (Fig. 3(a)-3(b) and column 5, lines 35-45); and

A fixed, active pixel border region permanently dedicated to displaying a border attribute (Figs. 3(a)-3(b) and column 5, lines 50-63), wherein said fixed, active pixel border region surrounds said rectangular pixel frame buffer region and comprises a width of less than 256 pixels (Figs. 3(a)-3(b) and column 5, lines 50-63);

A frame buffer memory (VRAM 3 is a frame buffer memory; see column 3, lines 60-61) for containing image data for generating an image within said frame buffer region (VRAM 3 is a frame buffer memory; see column 3, lines 60-61);

A border attribute register dedicated for containing border attribute (column 5, lines 50-63), wherein said border attribute is automatically selected to provide viewing contrast with image data located near said border region, and wherein said border attribute comprises color information for each pixel in said fixed, active pixel border region, and wherein said border attribute is equal to a background attribute currently being displayed (column 5, lines 50-63); and

A display controller coupled to said frame buffer memory (column 5, lines 10-15 a display controller controlling both the frame buffer memory-VRAM and the border region), coupled to receive said border attribute from said border attribute register (column 5, lines 50-63), and coupled to control said display panel, said display controller for generating a first set of signals for rendering said image within said frame buffer region and for generating a second set of signals for displaying said border attribute within said fixed, active pixel region (column 5, lines 50-63).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 10 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Canova et al. U.S. Patent No. 6,961,029 (hereinafter Canova).

1. Re Claims 1, 10 and 18:

Canova teaches a display unit (e.g., figures 1-2) comprising:

A display panel comprising a pixel matrix (e.g., Figs. 1A-1B and 7; column 7, lines 54-67 and column 8, lines 1-16) comprising:

A rectangular pixel frame buffer region (Fig. 10; column 7, lines 54-67 and column 8, lines 1-16); and

A fixed, active pixel border region permanently dedicated to displaying a border attribute (Figs. 1A-1B and 7), wherein said fixed, active pixel border region surrounds said rectangular pixel frame buffer region and comprises a width of less than 256 pixels (Figs. 1A-1B and 7 and column 2, lines 51-67; column 7, lines 54-67 and column 8, lines 1-16);

A frame buffer memory for containing image data for generating an image within said frame buffer region (Figs. 10 and 12 and column 2, lines 51-67 and column 3, lines 1-40; column 7, lines 54-67 and column 8, lines 1-16);

A border attribute register (dummy transistors of column 9, line 10 or a color filter pattern 520 for the dummy pixel border 312 of Figs. 10-12 and although the transistors are not active, the border region is a fixed and active pixel border region as the dummy pixels provide contrast improvement for increased viewability) dedicated for containing border attribute (column 9, lines 5-67), wherein said border attribute is automatically selected (e.g., column 2, lines 53-67 wherein the color of dummy pixels is automatically selected or white dummy pixels to provide

white border; see column 9, lines 23-24) to provide viewing contrast with image data located near said border region, and wherein said border attribute comprises color information for each pixel in said fixed, active pixel border region, and wherein said border attribute is equal to a background attribute currently being displayed (column 7, lines 54-67 and column 8, lines 1-16 and column 9, lines 5-67 wherein the both the border pixels and background pixels are white; column 9, lines 55-60; see column 8, lines 10-15 wherein the pixels of the pixel border 312 are generally displayed white to match the background pixel color and the dummy pixels contains respective color filters and dummy transistors are darkened; see column 9, lines 10); and

A display controller coupled to said frame buffer memory (Fig. 8 and column 8, lines 17-35), coupled to receive said border attribute from said border attribute register (Figs. 10 and 12, e.g., the dummy pixels remain darken or lit to provide black or white border), and coupled to control said display panel, said display controller for generating a first set of signals for rendering said image within said frame buffer region and for generating a second set of signals for displaying said border attribute within said fixed, active pixel region (column 7, lines 54-67 and column 8, lines 1-16 and column 9, lines 5-67).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla) and Dinwiddie et al. U.S. Patent No. 6,195,078 (hereinafter Dinwiddie).

4. Claim 1:

Matsuzaki teaches a display unit (e.g., figures 1-2) comprising:

A display panel comprising a pixel matrix comprising: a rectangular pixel frame buffer region (e.g., figures 6-7B; column 5, lines 25-60);

A fixed, active pixel border region permanently dedicated to displaying a border attribute, wherein said fixed, active pixel border region surrounds said rectangular pixel frame buffer region and comprises a width of less than 256 pixels (e.g., figures 6-7B; column 5, lines 25-60);

A frame buffer memory (VRAM 22) for containing image data for generating an image within said frame buffer region (figures 6-7B; column 5, lines 25-60);

A display controller (e.g., the display control circuit, SVGA 21 of figure 3) coupled to said frame buffer memory (e.g., VRAM 22), coupled to receive said border attribute from said border attribute register (e.g., the border producing circuit or registers of figures 1-3; column 5, lines 5-60; column 7, lines 10-65), and coupled to control said display panel (figures 1-7B; column 5, lines 5-60), said display controller for generating a first set of signals (i.e., pixel data) for rendering said image within said frame buffer region and for generating a second set of signals (i.e., border pixel data) for displaying said display attribute within said fixed, active pixel region (e.g., column 3, lines 6-25; column 7, lines 5-67; column 8, lines 1-35; column 13, lines 48-60).

However, it is remains to be shown whether Matsuzaki explicitly teaches a frame buffer memory. Matsuzaki teaches a VRAM for storing a frame of the image data (*Matsuzaki column 2, lines 10-15*) and a graphics control circuit fetching pixel data from VRAM 22 (*Matsuzaki figures 1-3; column 6, lines 3-65*) wherein VRAM 22 is a frame buffer memory.

It remains to be shown whether Matsuzaki teaches a border attribute register dedicated for containing said border attribute, wherein said border attribute is automatically selected to provide viewing contrast with image data located near said border region, and wherein said border attribute comprises color information for each pixel in said fixed, active pixel border region, and wherein said border attribute is equal to a background attribute currently being displayed.

Matsuzaki teaches selecting/switching one of the display formats including resolutions (*Matsuzaki column 2*); setting the format of the binary border pixel data in color values for the border pixels to be different from those for pixels within the effective display region (*Matsuzaki column 3 and 6-7*) and the format of the synthesized pixel data in the border section produced as 8-bit parallel data by the border producing circuit 25 synthesized with the pixel data from the binarizing half tone processing circuit 26 by the synthesizing circuit 27 (Matsuzaki column 3, 6-7) and therefore suggesting an obvious modification of Matsuzaki.

Matsuzaki teaches selecting/switching one of the display formats including resolutions (Matsuzaki column 2); setting the format of the binary border pixel data in **color values (color intensities) for the border pixels** to be different from those for pixels within the effective display region (Matsuzaki column 3 and 6-7) and thereby selecting the color values for the border area pixels surrounding the frame area image data to provide the viewing contrast. It is

noted that in Matsuzaki, the color values for the border area pixels is *automatically selected by the selecting/switching mechanism* to provide viewing contrast.

Kim teaches implicitly a frame buffer (*See Kim column 8, lines 55-67*). Furthermore, Singla teaches a display attribute being selected to provide viewing contrast with image data located near the border region (*e.g., Singla column 3, lines 28-50; column 5, lines 45-60*).

It would have been obvious to one of ordinary skill in the art to have incorporated the Kim's frame buffer and Singla's border region attribute setting method into Matsuzaki's display unit because Matsuzaki teaches a VRAM for storing image data (*Matsuzaki column 2, lines 10-15*) and a graphics control circuit fetching pixel data from VRAM 22 (*Matsuzaki figures 1-3; column 6, lines 3-65*) while Kim teaches a VRAM corresponds to a frame buffer memory (region). Moreover, Matsuzaki teaches selecting/switching one of the display formats including resolutions (*Matsuzaki column 2*); setting the format of the binary border pixel data in color values for the border pixels to be different from those for pixels within the effective display region (*Matsuzaki column 3 and 6-7*) and the format of the synthesized pixel data in the border section produced as 8-bit parallel data by the border producing circuit 25 synthesized with the pixel data from the binarizing half tone processing circuit 26 by the synthesizing circuit 27 (Matsuzaki column 3, 6-7) and therefore suggesting an obvious modification of Matsuzaki.

One having the ordinary skill in the art would have been motivated to incorporate the frame buffer of Kim because Kim teaches that the video frame buffer memory is constructed from VRAM (See Kim column 8, lines 55-67). One of the ordinary skill in the art would have been motivated to incorporate Singla's border region attribute setting method because Singla teaches a set of registers associated with a timing generator programmed to a particular attribute

including resolution (selectable resolution; Singla the Abstract column 5) and Singla further teaches border data set by a solid single-color surrounding the frame buffer image (changeable color; Singla column 8) and a display controller for user-selectable overriding of the predetermined border scheme to provide viewing contrast between the border region and the frame buffer region (changeable attributes; e.g., Singla the Abstract and column 10).

Although Matsuzaki, Kim and Singla does not explicitly disclose the claim limitation of "said display attribute is *automatically* selected to provide viewing contrast with image data located near said border region, wherein said display attribute comprises color and intensity information, and wherein said display attribute is equal to a background attribute", Dinwiddie discloses in column 9, lines 30-40 that the color data signal from the fringe palette 100 is *automatically* selected to provide the color for the fringe area around the OSD frame area and thereby the fringe color provides viewing contrast for the frame area. Moreover, Dinwiddie also discloses in column 11, lines 25-67 selecting a solid color byte from the fringe palette to provide the fringe color data for the fringe area surrounding the OSD frame area and controlling the extra bits to finger palettes and/or the attribute buffer with those extra bits controlling appropriate circuitry in the OSD system to generate those attributes. Therefore, Dinwiddie discloses the claim limitation of the display attribute being *automatically* selected to provide viewing contrast with image data (in the frame area).

Dinwiddie discloses in column 8, line 65 to column 9, line 18 that the attribute a ten bit entry from the fringe palette which produces a fringe color data signal containing three color component signals having three bits. The fringe palette of 512 colors (column 10, lines 5-15), each of the RGB intensities are represented by an 3-bit value. Therefore, Dinwiddie

discloses the claim limitation that the display attribute comprises color and intensity information (See also column 11, lines 61-65).

Dinwiddie discloses in column 10, lines 5-15 that background colors are selected from 512 possible colors and one fringe color is also selected from 512 possible colors. In addition, each palette entry in the foreground palette 42', the background palette 44' and the fringe palette 100 may be specified to appear as a solid color or a transparent overlay atop the received television image.

Applicant's claim limitation of "a background attribute" is any attribute, e.g., or a color attribute out from the 512 possible colors. Since Dinwiddie discloses one fringe color selected from the 512 possible colors, Dinwiddie has taught the fringe attribute being equal to one of the background attributes. Moreover, Dinwiddie discloses in column 11, lines 28-31 that the fringe palette 100 contains a single one byte entry corresponding to the portion of the palette 40" entry containing the background data, which contains a color data signal C and a solid color bit S. The solid color bit S, as selected from the 512 colors, is equal to one of the background solid color bit BG S, which is also selected from the same 512 colors.

Moreover, Matsuzaki suggests the claim limitation because Matsuzaki teaches selecting/switching one of the display formats including resolutions (Matsuzaki column 2); setting the format of the binary border pixel data in **color values (color intensities) for the border pixels** to be different from those for pixels within the effective display region (Matsuzaki column 3 and 6-7) and thereby selecting the color values for the border area pixels surrounding the frame area image data to provide the viewing contrast. It is noted that in Matsuzaki, the color

values for the border area pixels is *automatically selected by the selecting/switching mechanism* to provide viewing contrast.

Singla discloses border data set by a solid single-color surrounding the frame buffer image (changeable color; Singla column 8) and a display controller for user-selectable overriding of the predetermined border scheme to provide viewing contrast between the border region and the frame buffer region (changeable attributes; e.g., Singla the Abstract and column 10). Although Singla incorporates a user-selectable overriding of the border color data, the border color attribute is still being automatically selected by the display controller because once the user provides the color data, the display controller automatically selects the border color data to provide viewing contrast to the frame area image data.

One of the ordinary skill in the art would have been motivated to have *automatically* selected the border color attribute because it allows for the border color attribute to be set by the computer software and hardware in which the format of the binary border pixel data in color values for the border pixels is set to be different from those for pixels within the effective display region (Matsuzaki column 3 and 6-7) to provide viewing contrast and to provide changeable attribute to the border area pixels to provide controllable color attribute for the border region (Singla the Abstract and column 10).

5. Claim 2-4, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim), Yuri et al. U.S. Patent No. 5,805,149 (hereinafter Yuri), further in view of Ogawa et al. U.S. Patent No. 6,018,331 (hereinafter Ogawa) and Singla et al. U.S. Patent

No. 6,597,373 (hereinafter Singla) and Dinwiddie et al. U.S. Patent No. 6,195,078 (hereinafter Dinwiddie).

6. Claim 2-4, 8:

(1) The claim 2-4, 8 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of (1) the second set of signals being generated within invalid timing windows with respect to the frame buffer region; (2) a first portion of the second set of signals being generated x clock cycles before valid data for the frame buffer region commences and a second portion of the second set of signals being generated in an invalid horizontal timing window that ends x clock cycles after valid data for the frame buffer region; (3) a third portion of the second set of signals being generated in an invalid vertical timing window that commences x horizontal pulses before a first valid horizontal line commences of a frame and a forth portion of the second set of signals being generated in an invalid vertical timing window that ends x horizontal pulses after the end of the last valid horizontal line of the frame; (4) x being equal 2; (5) the frame buffer region comprising 160 rows and 160 columns of pixels.

As shown in the rejection of claim 1, Matsuzaki, Kim, Dinwiddie, and Singla teach the claimed invention of a display unit.

(2) However, it remains to be shown that Matsuzaki, Kim, Dinwiddie, Singla implicitly teach the additional claimed limitation as recited in claims 2-4.

(3) Singla, Ogawa and Yuri teaches the additional claimed limitation as recited in claims 2-4. Namely, Singla, Ogawa and Yuri teach the claimed limitation of (1) the second set of signals being generated within invalid timing windows with respect to the frame buffer region (Singla figures 2-5; Ogawa column 5, lines 4-67; column 6, lines 1-67; Ogawa figures 7-9; Yuri figure 7;

Ogawa teaches in Figures 7-9 frame writing intervals which correspond to the invalid timing intervals for generating the border frames); (2) a first portion of the second set of signals being generated x clock cycles before valid data for the frame buffer region commences and a second portion of the second set of signals being generated in an invalid horizontal timing window that ends x clock cycles after valid data for the frame buffer region (Singla figures 2-5; Ogawa column 5, lines 4-67; column 6, lines 1-67; Ogawa figures 7-9; Yuri figure 7; *Ogawa teaches in Figures 7-9 a first portion of the frame writing interval x clock cycles before the image writing interval and a second portion of the frame writing interval x clock cycles after the image writing interval*); (3) a third portion of the second set of signals being generated in an invalid vertical timing window that commences x horizontal pulses before a first valid horizontal line commences of a frame and a forth portion of the second set of signals being generated in an invalid vertical timing window that ends x horizontal pulses after the end of the last valid horizontal line of the frame (Singla figures 2-5; Ogawa column 5, lines 4-67; column 6, lines 1-67; Ogawa figures 7-9); 4) x being equal 2 (Ogawa figure 7; Singla figure 2; Yuri figure 7; *Ogawa teaches in Figures 7-9 a third portion of the frame writing interval x clock cycles before the image writing interval and a third portion of the frame writing interval x clock cycles after the image writing interval*); (5) the frame buffer region comprising 160 rows and 160 columns of pixels (Ogawa figure 7; Singla figure 2; Yuri figure 7). Moreover, Yuri further discloses in column 11-12 attributes including the gradation levels for the color palette, thus teaching other claim limitations set forth in the claim 2 as well including the display attribute comprises color and intensity information.

(4) It would have been obvious to one of ordinary skill in the art to have incorporated Singla, Ogawa and Yuri's timing generator into Matsuzaki/Kim/Dinwiddie/Yuri/Singla's display

device because Matsuzaki suggests partial rewrite driving using display start line address, the number of continuous display lines, the total number of lines, the total number of pixels, and the border region to the line address producing circuit, thereby obtaining partial display information (Matsuzaki column 8, lines 1-67). Matsuzaki discloses a plurality of display formats for the effective display region (Matsuzaki column 8, lines 1-67). Therefore the claimed limitation suggests an obvious modification of Matsuzaki/Kim/Dinwiddie/Yuri/Singla.

(5) One having the ordinary skill in the art would have been motivated to do this because Ogawa teaches timing chart for the horizontal/vertical timing intervals to generate the timing signals so that the input image signal is displayed in the center and its periphery is made a frame, the drive of picture elements corresponding to the frame can be carried out during the horizontal/vertical blanking intervals (Ogawa column 5, lines 4-67; column 6, lines 1-67; Yuri figure 7).

7. Claim 5, 6, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim) and Yuri et al. U.S. Patent No. 5,805,149 (hereinafter Yuri) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla) and Dinwiddie et al. U.S. Patent No. 6,195,078 (hereinafter Dinwiddie).

Claim 5:

The claim 5 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the display attribute of the border region comprising a color attribute and an intensity attribute. However, Matsuzaki further discloses the claimed limitation of the display

attribute of the border region comprising a color attribute and an intensity attribute (e.g., Matsuzaki figures 6-8). Dinwiddie discloses in column 8, line 65 to column 9, line 18 that the attribute a ten bit entry from the fringe palette which produces a fringe color data signal containing three color component signals having three bits. The fringe palette of 512 colors (column 10, lines 5-15), each of the RGB intensities are represented by an 3-bit value. Therefore, Dinwiddie discloses the claim limitation that the display attribute comprises color and intensity information (See also column 11, lines 61-65).

Claim 6:

The claim 6 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the display panel being a thin film transistor liquid crystal display panel. However, Matsuzaki further discloses the claimed limitation of the display panel being a thin film transistor liquid crystal display panel (e.g., Matsuzaki column 1, lines 20-60; column 5, lines 1-25).

Claim 9:

The claim 9 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of background display attribute register. Matsuzaki further discloses the claimed limitation of background display attribute register (e.g., Matsuzaki figures 6-8).

8. Claims 10-14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of in view of Kim et al.

U.S. Patent No. 5,355,443 (hereafter Kim), and further in view of Ogawa et al. U.S. Patent No. 6,018,331 (hereafter Ogawa) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla) and Dinwiddie et al. U.S. Patent No. 6,195,078 (hereinafter Dinwiddie).

9. Claim 10:

The claim 10 encompasses the same scope of invention as that of claims 1 and 2. The claim 10 is rejected for the same reasons set forth in claims 1 and 2.

Claims 11-12:

The claim 11, or 12 encompasses the same scope of invention as that of claims 1-4. The claim 11 is rejected for the same reasons set forth in claims 1-4.

Claim 13:

The claim 13 encompasses the same scope of invention as that of claims 1-5. The claim 13 is rejected for the same reasons set forth in claims 1-5.

Claim 14:

The claim 14 encompasses the same scope of invention as that of claims 1-6. The claim 14 is rejected for the same reasons set forth in claims 1-6.

Claim 16:

The claim 16 encompasses the same scope of invention as that of claims 1-8. The claim 16 is rejected for the same reasons set forth in claims 1-8.

Claim 17:

The claim 17 encompasses the same scope of invention as that of claims 1-9. The claim 16 is rejected for the same reasons set forth in claims 1-9.

10. Claims 18-23 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim) and Yuri et al. U.S. Patent No. 5,805,149 (hereinafter Yuri), further in view of Ogawa et al. U.S. Patent No. 6,018,331 (hereafter Ogawa) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla), Dinwiddie et al. U.S. Patent No. 6,195,078 (hereinafter Dinwiddie), and He et al. U.S. Patent No. 6,323,849 (He).

Claims 18-23:

The claim 18-23 encompasses the same scope of invention as that of claims 1-9 except additional claimed limitation of a handheld device. Although the "handheld device" appears in the preamble, the term "handheld" cannot be found in the body of the claim. Nevertheless, the display device as disclosed in Matsuzaki, or Kim, or Yuri, or Ogawa or Singla or Dinwiddie is a proper sized display device as far as portability is concerned and thus is a handheld device. Moreover, He/Yuri explicitly discloses the additional claimed limitation of a handheld device (He column 1, lines 20-35; Yuki column 14, lines 1-15). It would have been obvious to one of the ordinary skill in the art to have made the display device of Matsuzaki, or Kim, or Yuri, or Ogawa or Singla or Dinwiddie portable/handheld because these references teaches proper sized display devices. One of the ordinary skill in the art would have been motivated to do so to incorporate the display devices to PDA's, personal games and palm-sized computers (He column 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (571) 272-7665. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jcw